Stoneman
#31a
2-7-01

PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of:

TOMITA et al.

Group Art Unit: Unassigned

Divisional of Parent
Application No.: 09/240,007

Examiner: Unassigned

Filed: Herewith

Attorney Dkt. No.: 100353-00029

For: SEMICONDUCTOR DEVICE RECONCILING DIFFERENT TIMING SIGNALS

PRELIMINARY AMENDMENT

Commissioner for Patents
Washington, D.C. 20231

Date: December 12, 2000

Sir:

Prior to initial examination of the application, please amend the above-identified application as follows:

IN THE CLAIMS:

Please cancel claims 1-42.

Please add new claims 43-48 as follows:

--43. A memory circuit, comprising:

an address-input circuit which latches address signals in response to a clock signal, and outputs the address signals in response to the clock signal, said address-input circuit includes a delay circuit which operates in response to the clock signal;

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